Electronic Version
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METHOD FOR IMPLEMENTING ADVANCED ENCRYPTION STANDARDS USING A VERY LONG INSTRUCTION WORD ARCHITECTURE PROCESSOR

Abstract

A method for implementing Advanced Encryption Standards (AES) by a very long instruction word (VLIW) architecture processor. The method includes inputting the instructions for AES into the processor, decoding and scheduling the input instructions, controlling at least one of a plurality of multiplexers to output data from a first register of the processor and/or an arithmetic logic unit to the first register and/or the arithmetic logic unit according to the decoded and scheduled instructions, controlling the arithmetic logic unit to perform operations, and outputting results of the operations to the plurality of the multiplexers.